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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	09/995,031	AMOS ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7-11 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-11 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7-11, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suguro (US Pat. 6,476,545) in view of Talwar et al. (US Pat. 6,300,208, hereinafter Talwar) and Huang et al. (US Pat. 6, 248,673, hereinafter Huang).

Regarding claims 1, 2, 10, 11, and 17, Figure 2C of Suguro discloses a MOSFET comprising: a semi-conducting substrate 11 having source and drain regions (not shown but inherent); a gate dielectric layer 13 made of HfO_2 (col. 6, lines 37-40); and a gate 15 formed of Mo or W (col. 6, lines 44-48) on top of said gate dielectric. Suguro does not explicitly disclose the thickness of the gate dielectric is less than 50 angstroms. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Suguro by using a thickness less than 50 angstroms, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The ordinary artisan would have been motivated to modify Suguro in the manner described above for the purpose of increasing the integration density (by forming smaller devices).

A further difference between Suguro and the claimed invention is the gate electrode comprises Re. Figure 2H of Talwar discloses a MOSFET device comprising a gate electrode 9

made of Re, Mo, or W (col. 5, lines 46-50). Therefore, Talwar implicitly discloses that Re, Mo, and W can be equivalently used for the same purpose. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Suguro by using Re as the gate electrode for the purpose of selecting an equivalent material that is known in the art to be used for the same purpose (see MPEP 2144.06).

A further difference between Suguro and the claimed invention is the gate has an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}. Huang discloses annealing a MOSFET in a hydrogen environment at a temperature of about 350 ° C at a pressure of about 700 torr (col. 8, lines 21-46 of Huang). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Suguro by using the hydrogen anneal process of Huang for the purpose of stabilizing interface states and trapped charges (col. 8, lines 54-57 of Huang). After performing the hydrogen anneal taught by Huang, it is inherent that the trapped charge density will be about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}.

Regarding claims 7-9 and 14-16, Suguro does not specifically disclose the material of the semiconductor substrate. However, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Suguro by using an n or p-type silicon substrate, such as that taught by Talwar (col. 4, lines 39-41 and col. 5, lines 6-10 of Talwar) for the purpose of selecting a well-known, inexpensive semiconductor material.

Claim 1, 2, 7-11, and 14-16 are rejected under 35 U.S.C. 103(a) as being obvious over Deshpande et al. (US PGPub 2003/0011080, hereinafter Deshpande) in view of Talwar and Huang.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claims 1, 2, 7-11, and 14-16, Figure 1F of Deshpande discloses a semiconducting substrate 10 (n or p-type silicon) (paragraph [0036]) having source and drain regions 20; a gate dielectric 12 on said semiconductor substrate, said gate dielectric is zirconium oxide (paragraph [0039]); and a gate formed of Pt or Ir (paragraph [0040]). Deshpande discloses the gate dielectric has a thickness of 15-100 angstroms (paragraph [0039]). Since the claimed

range overlaps the range disclose by the prior art, a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USQP2d 1934 (Fed. Cir. 1990).

A difference between Deshpande and the claimed invention is the gate electrode comprises Re. Figure 2H of Talwar discloses a MOSFET device comprising a gate electrode 9 made of Re, Pt, or Ir (col. 5, lines 46-50). Therefore, Talwar implicitly discloses that Re, Pt, and Ir can be equivalently used for the same purpose. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Deshpande by using Re as the gate electrode for the purpose of selecting an equivalent material that is known in the art to be used for the same purpose (see MPEP 2144.06).

A further difference between Deshpande and the claimed invention is the gate has an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}. Huang discloses annealing a MOSFET in a hydrogen environment at a temperature of about 350 ° C at a pressure of about 700 torr (col. 8, lines 21-46 of Huang). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Deshpande by using the hydrogen anneal process of Huang for the purpose of stabilizing interface states and trapped charges (col. 8, lines 54-57 of Huang). After performing the hydrogen anneal taught by Huang, it is inherent that the trapped charge density will be about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}.

Claim 1, 2, 7-11, and 14-17 are rejected under 35 U.S.C. 103(a) as being obvious over Lee et al. (US Pat. 6,614,079, hereinafter Lee) in view of Talwar and Huang.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claims 1, 2, 7-11, and 14-17, Figure 1 of Lee discloses a semiconducting substrate 10 (n or p-type silicon) (col. 5, lines 15-22) having source and drain regions 11; a gate dielectric 14 on said semiconductor substrate, said gate dielectric is HfO_2 (col. 5, lines 55-58) and a gate formed of Pt or Ir (col. 6, lines 1-3). Lee discloses the gate dielectric has a thickness of 15-100 angstroms (col. 5, lines 48-50)). Since the claimed range overlaps the range disclose

by the prior art, a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USQP2d 1934 (Fed. Cir. 1990).

A difference between Lee and the claimed invention is the gate electrode comprises Re. Figure 2H of Talwar discloses a MOSFET device comprising a gate electrode 9 made of Re, Pt, or Ir (col. 5, lines 46-50). Therefore, Talwar implicitly discloses that Re, Pt, and Ir can be equivalently used for the same purpose. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Lee by using Re as the gate electrode for the purpose of selecting an equivalent material that is known in the art to be used for the same purpose (see MPEP 2144.06).

A further difference between Lee and the claimed invention is the gate has an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}. Huang discloses annealing a MOSFET in a hydrogen environment at a temperature of about 350 ° C at a pressure of about 700 torr (col. 8, lines 21-46 of Huang). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Lee by using the hydrogen anneal process of Huang for the purpose of stabilizing interface states and trapped charges (col. 8, lines 54-57 of Huang). After performing the hydrogen anneal taught by Huang, it is inherent that the trapped charge density will be about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be

reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew C. Landau

April 19, 2007

KENNETH PARKER
SUPERVISORY PATENT EXAMINER